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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,898	03/30/2004	Motoki Kanamori	XA-10067	1325

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
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EXAMINER	
VO, THANH DUC	
ART UNIT	**PAPER NUMBER**
2189	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/811,898	KANAMORI ET AL.	
	Examiner	Art Unit	
	Thanh D. Vo	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,6,7 and 10* is/are rejected.

7)☒ Claim(s) *3,5,8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the Request for Reconsider of the Final Rejection filed on February 1, 2007. Claims 1-10 are currently pending.

2. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

3. This Office Action will supercede the previous Office Action submitted on November 1, 2006. The claims are being rejected as follow:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1, 2, 4, 6, and 7 are rejected under 35 U.S.C. 102(a) as being anticipated by Kawai et al. (US Pub. 2003/0090953).

As per claim1, Kawai et al. discloses a memory card conforming to a first operation standard (Fig. 5, second operation mode), a second operation standard (Fig. 5, first operation mode), and a third operation standard (Fig. 5,

third operation mode) based on the first operation standard (Fig. 5, second operation mode, wherein second operation mode is MMC and third operation mode is HS-MMC based on the terminal configurations), comprising:

a non-volatile semiconductor memory (Fig. 1) having a plurality of semiconductor memory cells, wherein each said memory cell is capable of storing information, and

a controller that executes operation instructions to the non-volatile semiconductor memory based on the received commands (page 4, paragraph 0043), wherein:

the controller controls a first data output timing that satisfies the first operation standard (Fig. 5, second operation mode) and the second operation standard (Fig. 5, first operation mode), in a first operation mode (paragraph 0073, lines 3-7, wherein first operation mode is equivalent to the first operation standard), and controls a second data output timing that satisfies the third operation standard (Fig. 5, third operation mode), in a second operation mode (paragraph 0073, lines 5-7).

Additional comprehensive memory card operation of Kawai et al. related to data output and timing is further disclosed on paragraph 0066.

As per claim 2, Kawai et al. discloses a memory card, wherein:

the controller includes a data timing switching unit that outputs data at a fall edge of a clock signal in the first data output timing, and outputs data at a rise edge of a clock signal in the second data output timing (page 5, paragraph

0059, wherein data timing switching unit is an inherent feature of Kawai et al. since a clock signal has to alternate from fall edge to rise edge and so on).

As per claim 4, Kawai et al. discloses a memory card, wherein:

the controller includes a timing delay switching unit (Fig. 1, item 10, timing adjusting circuit) that outputs data at a first delay time at the first data output timing, and outputs the data at a second delay time being shorter than the first delay time at the second data output timing (page 5, paragraph 0058, wherein the clock is delayed to synchronize with the data output therefore one of the delayed time is shorter than the other delayed time).

As per claim 6, Kawai et al. discloses a memory card, wherein:

the controller includes a data output time switching unit that switches a rise time/fall time of the data in the first data output timing, so that the rise time/fall time of the data becomes shorter to the first data output timing (see page 5, paragraph 0058-0059, wherein the clock is delayed/switched to synchronize with the data output timing).

As per claim 7, Kawai et al. discloses a memory card, wherein the data output time switching unit includes:

a timing register to which one of the first data output timing and the second data output timing is set (See Fig. 10 and corresponding figure

description on page 4 paragraph 0051, wherein the output clock signal/timing is set by plurality of delayed clock);

an output buffer (Fig. 1, item 9) that outputs data on the basis of an output data enable signal (Fig. 6, item 403, dat_oe_0-3), when one of the first data output timing and the second data output timing is set to the timing register (page 4, paragraph 0051, and Fig. 10, wherein the first and second data output timing is set at the time adjusting circuitry),

an auxiliary output buffer (Fig. 6, item 26s) that outputs data on the basis of the output data enable signal (Fig. 6, item 403, dat_oe_0-3) at the second data output timing, and

an auxiliary output buffer enable unit that outputs the output data enable signal to the auxiliary output buffer, when the second data output timing is set to the timing register. See page 6, paragraph 0066 and Fig. 6 and 10, wherein the data is output at its output timing as the time the output enable signal is enabled.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai et al. (2003/0090953) in view of Yagishita (2002/0145935 A1).

As per claim 10, Kawai et al. disclosed non-volatile semiconductor memory (flash memory, Fig. 1, item 2, page 4, paragraph 0043, lines 2-3).

Kawai et al. did not specifically disclose a controller controls the plural non-volatile semiconductor memories arbitrarily in parallel operation in correspondence with the parameter value set to the power consumption parameter register.

Yagishita disclosed a power consumption and operation frequency in a circuitry wherein the lowering the operation frequency will reduce the power consumption; hence, they are operating in parallel (See Abstract, lines 11-12; and page 1, paragraph 0010, lines 6-13). Power consumption parameter register is readily apparent to one having an ordinary skill in the art since a register to hold the power consumption value is a required feature in a circuitry. Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to recognize that the power consumption is being controlled in corresponding to (or in parallel to) the operation requirement such as the nonvolatile memories in order to supply enough of voltage and current to perform the operation without error while increasing the efficiency.

Allowable Subject Matter

6. Claims 3, 5, 8, and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments filed August 7, 2006 have been fully considered but they are not persuasive.

Applicant indicated that neither Kawai et al. nor Yagishita et al. discloses or suggests a third operation. However, Kawai et al. clearly disclosed a third operation standard in Fig. 5.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh D. Vo whose telephone number is (571) 272-0708. The examiner can normally be reached on M-F 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thanh D. Vo
Patent Examiner
AU 2189
04/16/2007

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